

FIG. 1A
(PRIOR ART)

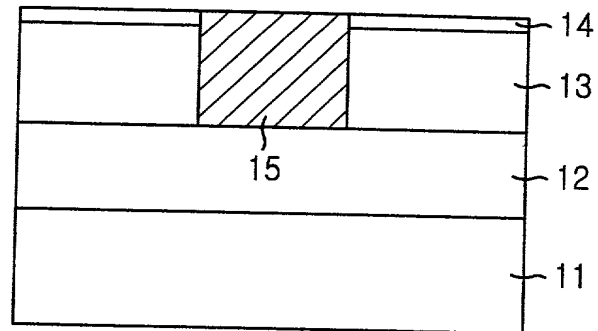


FIG. 1B
(PRIOR ART)

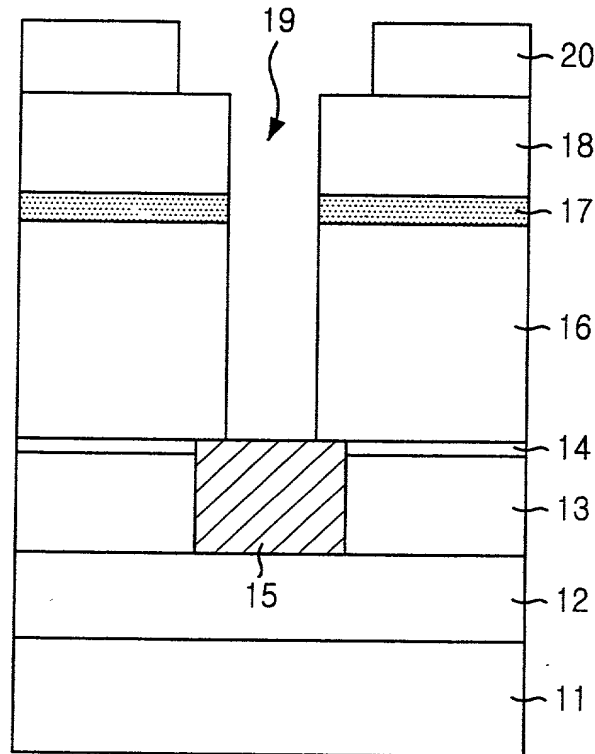


FIG. 1C
(PRIOR ART)

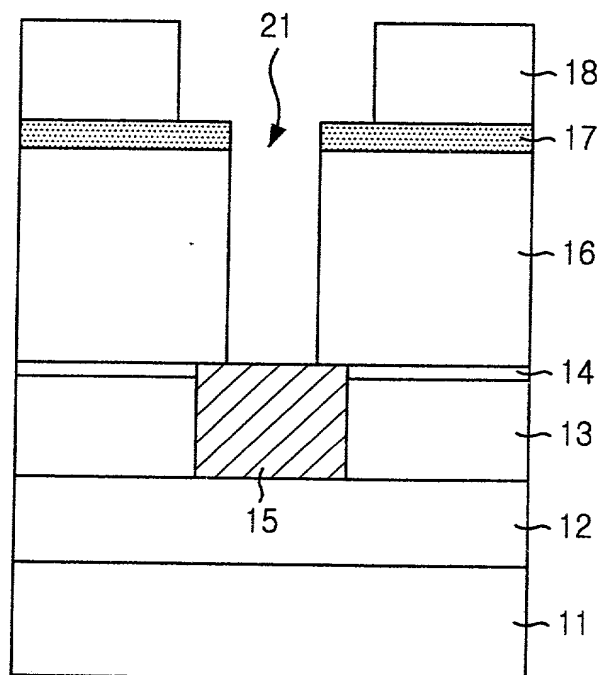


Fig. 1 is a cross-sectional view of a semiconductor device. The device is formed on a substrate 11. A base layer 12 is formed on the substrate 11. A gate layer 13 is formed on the base layer 12. A gate electrode 14 is formed on the gate layer 13. A gate insulating layer 15 is formed on the gate electrode 14. A gate contact layer 16 is formed on the gate insulating layer 15. A gate contact pad 17 is formed on the gate contact layer 16. A gate contact pad 18 is formed on the gate contact pad 17. A gate contact pad 22 is also shown, with a gate contact pad 22a.

FIG. 2A
(PRIOR ART)

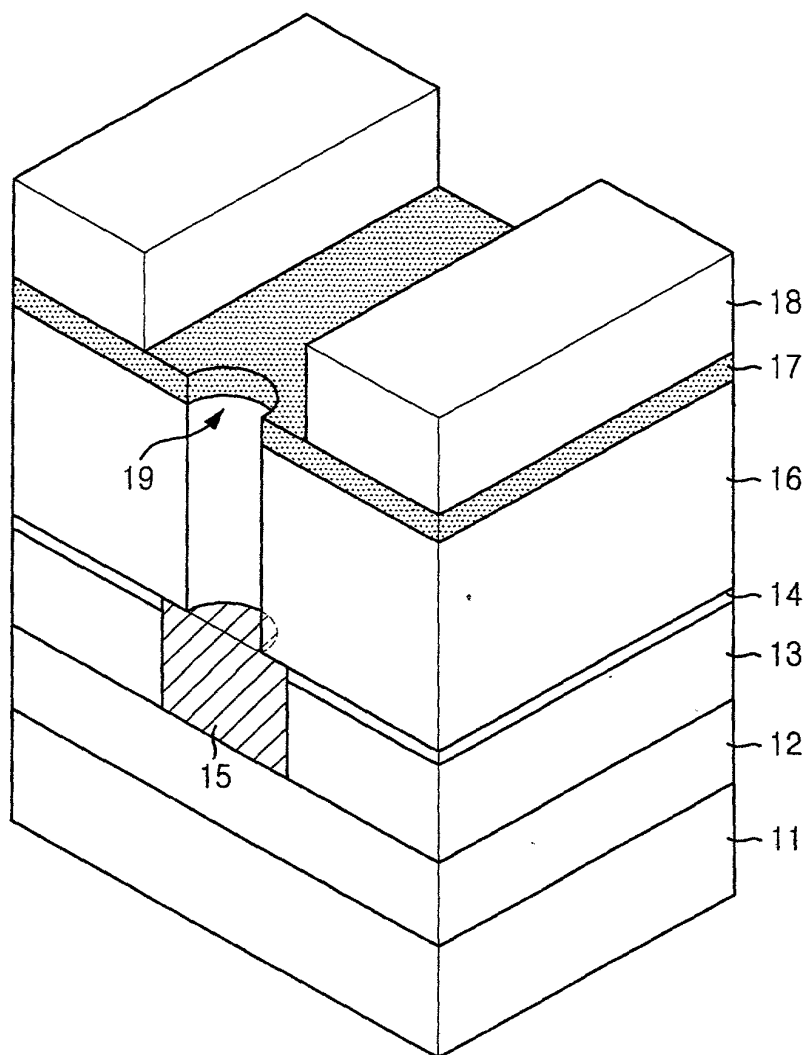


FIG. 2B
(PRIOR ART)

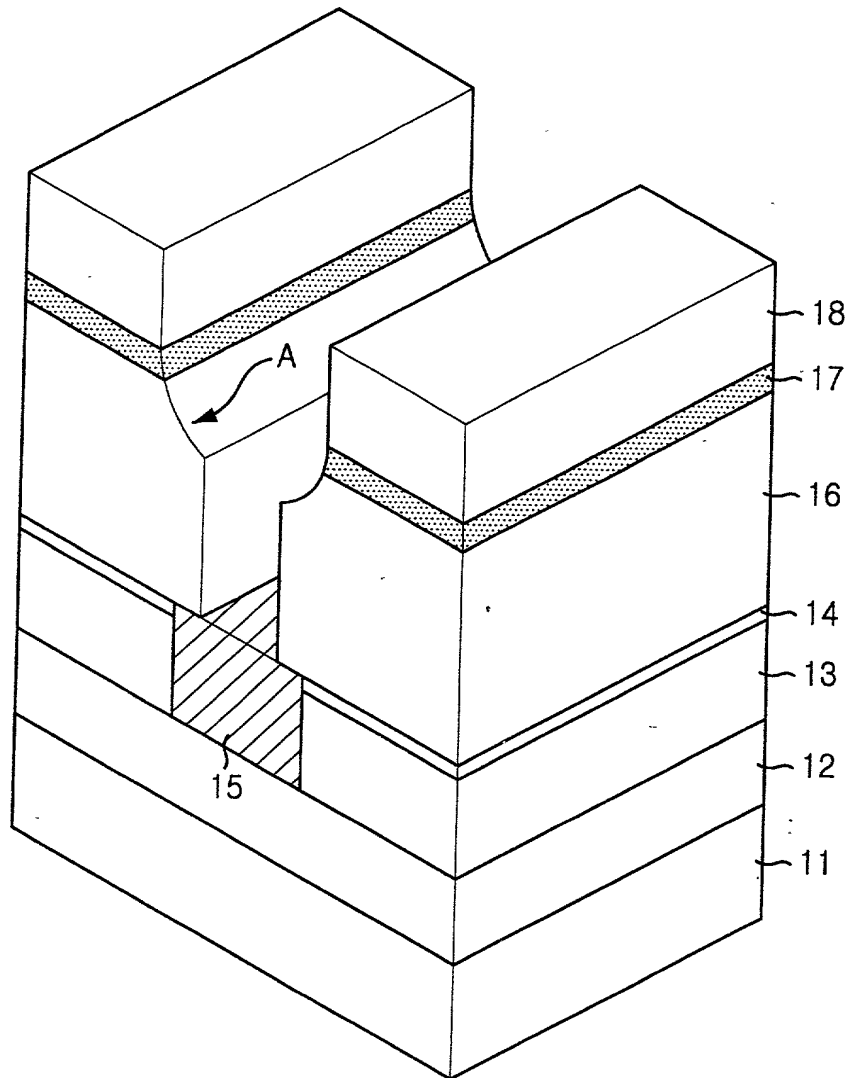


FIG. 3A

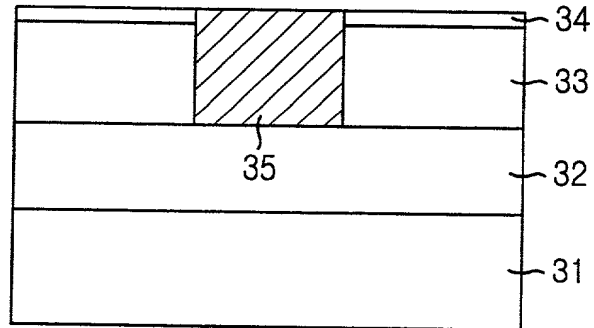


FIG. 3B

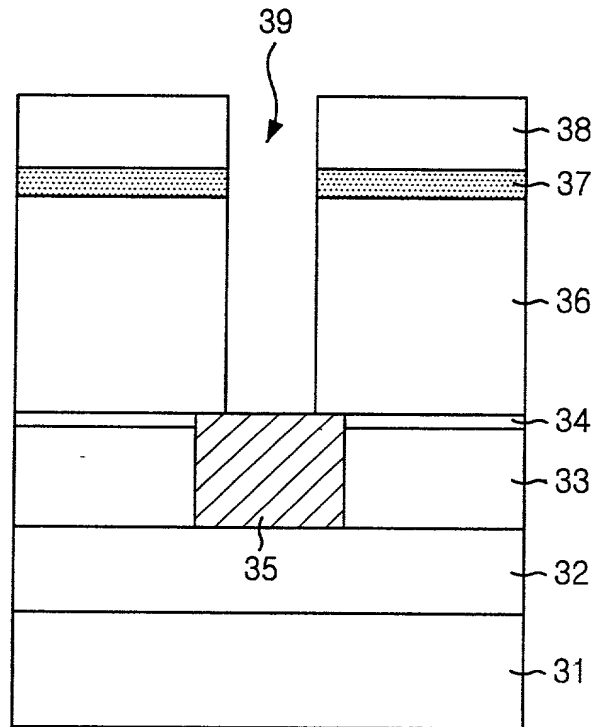


FIG. 3C

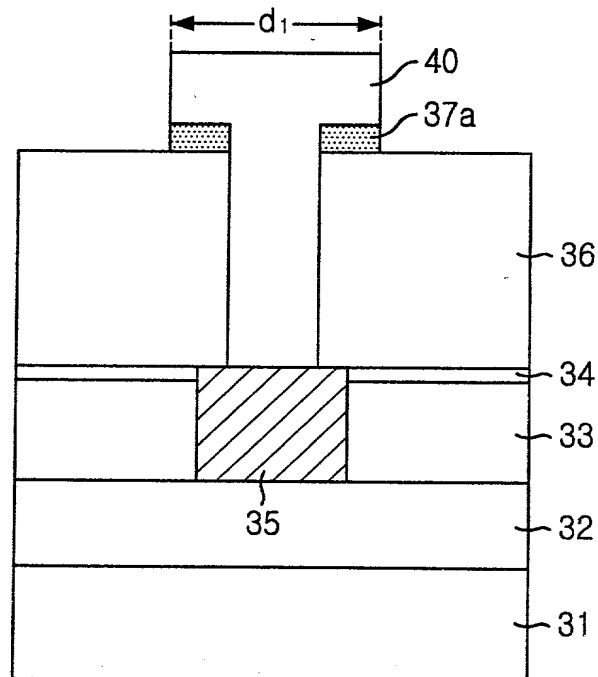


FIG. 3D

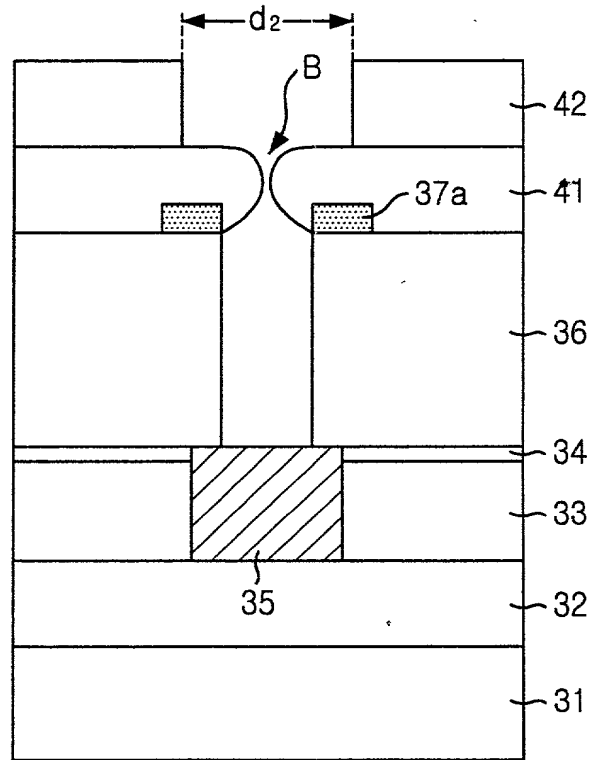


FIG. 3E

